Amendments to the Claims

This listing of the Claims will replace all prior versions and listings of the claims in this patent application.

Listing of the Claims

1-32. (canceled)

33. (original) An embedded DRAM and capacitor structure device comprising:

trenched capacitors in two twisted trenches through an insulating layer in a memory area of an integrated circuit wherein said two twisted trenches are mirror images of each other and wherein each capacitor in a first of said two twisted trenches is horizontally aligned with a capacitor in a second of said two twisted trenches to form pairs of capacitors wherein said pairs of capacitors are separated from each other horizontally by a first or a second distance wherein said first distance is greater than said second distance;

a bit line contact in said memory area through said insulating layer to a bit line wherein said bit line contact lies between said two twisted trenches and in a horizontal line with one capacitor pair wherein said one capacitor pair has said first separation distance and adjacent capacitor pairs have said second separation distance; and

first line metal contacts in a logic area of said integrated circuit;

wherein said bit line contact and said first line metal contacts are no higher vertically than said trenched capacitors.

34. (new) A DRAM structure comprising:

trenched capacitors in a trench through an insulating layer in a memory area, wherein each of said trenched capacitors comprises a bottom electrode lining an opening in said insulating layer , a capacitor dielectric layer disposed on said bottom electrode , and a top electrode disposed on said capacitor dielectric layer wherein an opening remains in said top electrode within said trench; and

a conductive line disposed on said top electrodes and filling inside said opening and said trench continuously wherein said conductive line is no higher vertically than said top electrode.

35. (new) The DRAM structure according to claim 34, further comprising a bit line contact in said memory area through said insulating layer to a bit line.

36. (new) The DRAM structure according to claim 34, wherein said bit line contact is no higher vertically than said trenched capacitors.

37. (new) The DRAM structure according to claim 34, wherein said insulating layer is a laminated layer comprising a stop layer, an insulating oxide layer, a silicon carbide layer, and a low-K layer disposed sequentially over said memory area.

38. (new) The DRAM structure according to claim 37, wherein said trench is formed in said low-K layer and does not exceed said silicon carbide layer .

39. (new) The DRAM structure according to claim 37, wherein said bottom electrode is in contact with said stop layer.

40. (new) The DRAM structure according to claim 34, wherein said trench is twisted-shaped.

41. (new) A DRAM structure, comprising:

trenched capacitors in two trenches through an insulating layer in a memory area; and

two conductive lines filling said two trenches respectively and continuously in contact with said trenched capacitors; and

a bit line contact in said memory area through said insulating layer to a bit line wherein said bit line contact lies between said two trenches;

wherein said bit line contact is no higher vertically than said trench capacitors.

42. (new) The DRAM structure according to claim 41, wherein each of said trenched capacitors comprises a bottom electrode layer lining an opening in said insulating layer, a capacitor dielectric layer disposed on said bottom electrode, and a top electrode layer disposed on said capacitor dielectric layer.

43. (new) The DRAM structure according to claim 42, wherein said conductive lines are disposed on said top electrode layers and substantially filling inside said openings and said trenches respectively wherein said conductive lines are no higher vertically than said top electrode layers.

44. (new) The DRAM structure according to claim 42, wherein said insulating layer is a laminated layer comprising a stop layer, an insulating oxide layer, a silicon carbide layer, and a low-K layer , disposed sequentially over said memory area.

45. (new) The DRAM structure according to claim 44, wherein said trenches are formed in said low-K layer and do not exceed said silicon carbide layer.

46. (new) The DRAM structure according to claim 44, wherein said bottom electrodes contact said stop layer.

47. (new) The DRAM structure according to claim 41, wherein said trenches are twisted-shaped.

48. (new) An embedded DRAM and capacitor structure device, comprising:

trenched capacitors in two trenches through an insulating layer in a memory area of an integrated circuit;

a bit line contact in said memory area through said insulating layer to a bit line wherein said bit line contact lies between said two trenches; and

first line metal contacts in a logic area of said integrated circuit;

wherein said bit line contact and said first line metal contacts are no higher vertically than said trenched capacitors.

49. (new) The embedded DRAM and capacitor structure device according to claim 48, further comprising two conductive lines filling said two trenches respectively and continuously in

contact with said trenched capacitors wherein said two conductive lines are no higher vertically than a top electrode of said trenched capacitors.

50. (new) The embedded DRAM and capacitor structure device according to claim 48, wherein said two trenches are twisted-shaped.

51. (new) The embedded DRAM and capacitor structure device according to claim 50, wherein said two twisted trenches are mirror images of each other.

52. (new) The embedded DRAM and capacitor structure device according to claim 50, wherein each capacitor in a first of said two twisted trenches is horizontally aligned with a capacitor in a second of said two twisted trenches to form pairs of capacitors wherein said pairs of capacitors are separated from each other horizontally by a first or a second distance wherein said first distance is greater than said second distance.

53. (new) The embedded DRAM and capacitor structure device according to claim 52, wherein said bit line contact is in a horizontal line with one capacitor pair wherein said one capacitor pair has said first separation distance and adjacent capacitor pairs have said second separation distance.